KARTHIK KURUDI RAMAKRISHNA

Personal Details

Date of Birth:	09 May, 1997	E-mail:	karthik.rampad@gmail.com
Phone:	+91 948 396 1197	LinkedIn:	linkedin.com/in/karthik-kr
Place:	Bangalore, Karnataka, India	Website:	www.karthikkr.com

Work Experience

Analog Devices, Bangalore

Current
Apr 2021

Engineer, Design Verification Engineering (Grade P2)

- Developing a Universal Config Interface to provide a common platform for pre-silicon verification of test cases and post-silicon evaluation of test-cases.
- Working on a software API that translates a test-suite written in higher level language into a pre-silicon testbench stimulus or post-silicon wire toggles based on the configuration.
- Built Testbench Infrastructure to model system behavior for real-life testbench stimulus and analysis mechanisms.
- Working with architecture and applications team to accurately model the devices to replicate system level behaviour with accuracy.
- Previous work on Apollo MxFE involved Developing Verification Plans, Building UVM Testbench, Writing Test Sequences, Analyzing Coverage, including Functional and Code Coverage.
- Verified design at system level using directed tests and various connectivity checks using Formal Verification Methodology.
- Worked on Constrained-random Verification at block level inside AMSD environment and directed tests at subsystem.
- Verified complex features at subsystem and system level by leveraging RTG infrastructure.

Mar 2021
April 2020

Engineer, Design Verification Engineering (Grade P1)

- Performed Datapath Verification for 5G NR stimulus on Emulation platform.
- Used python helper scripts and Matlab modeling to generate test suitable data.
- Introduced Datapath level NR verification using band data.
- Debugged Digital and Analog Register Access issues using Universal Verification Methodology (UVM) based tests

Mar 2020
July 2019

Engineer, Design Verification Engineering (Co-op)

- Completed Interrupt verification, Register Access using a UVM testbench.
- Applied Formal Verification tools for System Level Verification
- Performed subsystem level AHB Protocol verification, and Control Status Register verification.

Tools

- Cadence Tool Suite (Xcelium, Simvision, IMC)
- JasperGold Formal Verification Apps (FPA, Connectivity Verification, Unreachability Analysis)
- MATLAB
- Octave
- Electric & LT Spice

Programming Languages

- C
- C++
- C#
- Python
- Verilog
- System Verilog
- Java

Education

Present 2021	M.Tech. (Dept. of Electrical Engineering), **Indian Institute of Technology Madras** Trimester 7 - Specializing in Communications and Signal Processing
June 2019	B.E. (Electronics & Communication), **BMS College Of Engineering**, Bangalore CGPA: **9.71/10** (III Rank Holder in Dept of ECE - 2019)
June 2015	Pre-University Course (PUC), **Sri Bhagawan Mahaveer Jain College**, Bangalore Percentage: **96.00%** (KVPY Rank SX: AIR 579 KCET Engineering: 297)
May 2013	10th (ICSE), **Deccan International School**, Bangalore Percentage: **94.83%** (Academic Excellence Awardee)

Other Accomplishments

- Presented and Co-Authored a Paper of DV of Apollo MxFE and won the Best Paper Award
- Co-Authored a Paper on DV to validate 5G NR parameters and won Best Paper Award
- Led the Young Proffesional Network's Newsletter team and mentored the team to move to a paperless format, under the green initiative.
- Officially Ordained as Quizmaster for quizzes held throughout the year.